REMARKS

Applicants have reviewed the comments and rejections set forth by the Examiner in the Office Action dated July 12, 2005 and respectfully respond with the amendments above and the following remarks.

Claims 8-9, 16, 20-27 and 29-30 are pending in the present case. Claims 8-9, 16 and 20 are amended herein. Claims 6-7, 14-15, 17-19 and 28 have been previously cancelled. No new matter is added. Applicants respectfully request reconsideration in view of the above amendments and the arguments set forth below.

CLAIM REJECTIONS

Claims 8, 9, 25 and 26, Claims 16 and 23-24, Claims 20 and 21-22, and Claims 27 and 29-30 are rejected under 35 USC 102(e) over US Patent No. 6,762,466 B2 to Huang, et al. (hereinafter Huang). Applicants have reviewed the reference cited and respectfully assert it does not teach or suggest the embodiments of the present invention as recited in Claims 8, 9, 25 and 26, Claims 16 and 23-24, Claims 20 and 21-22, and Claims 27 and 29-30 for the following rationale.

As Applicants understand the reference, Huang teaches "a circuit structure for connecting the bonding pad of a semiconductor device with an electrostatic discharge (ESD) protection circuit ..." and to do so such "that line width of the conductive connection wire can be reduced, thereby increasing the manufacturing process window." Huang, col. 2, ll. 15-24. Huang expressly teaches that the multiple current carrying pathways therein allow smaller "line widths" allow "more flexibility in circuit design," (Id. at ll. 52-54) and to allow continuing ESD protection even "when one of

these [conductors] is accidentally severed." (Id. at ll. 56-59). The teaching of Huang thus differs from the embodiments of the present invention recited in Claims 8-9 and 25-26.

Claims 9, 25 and 26 depend on independent Claim 8. As amended herein, Claim 8 reads as follows, with underlining added for emphasis:

> 8. A semiconductor structure comprising:
> a pad area;
> an electrostatic discharge protective device disposed directly below said pad area, said electrostatic discharge protective device comprising a transistor and a resistance, wherein said pad area comprises:
> a substrate;
> a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal; and
> a second layer of metal disposed above said first layer of metal;
> a layer of dielectric disposed between said first metal layer and said second metal layer; and
> a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias, wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another and wherein a resistive value of said resistance is configured during a process for fabricating said semiconductor structure, wherein said resistive value of said resistance is fixed therein with setting a particular number for said portion of said plurality of individual vias in parallel <u>and wherein said setting tunes said electrostatic discharge protective device for performing an electrostatic discharge protective function</u>.

Independent Claims 16, 20 and 27 are amended herein after a similar fashion.

Claims 9, 23-24, Claims 20-22, and Claim 29-30 respectively depend on independent Claims 8, 16, 20 and 27.

Claims 8, 16, 20 and 27, as amended herein, recite that a semiconductor structure has an electrostatic discharge protective device (hereinafter ESPD) disposed directly below a pad area thereof. The semiconductor structure also has a via, comprising a plurality of individual vias arranged in parallel, which comprise a portion of the resistance of the ESPD. The resistive value corresponding to the ESDP resistance is configured during fabrication of the semiconductor structure, with setting a particular number of the individual vias in parallel. So setting this number of parallel individual vias tunes the electrostatic discharge protective device for performing its function.

As described in the original specification from lines 9-14 at page 11, in embodiments of the present invention recited in Claims 8, 16, 20 and 27, setting the resistive value of the ESPD resistance to be readily configured during fabrication of the semiconductor structure with setting a particular number of the individual vias allows tuning of junctions therein, of the ESDP network formed therewith, and of the ESDP device itself, for instance, the resistive-capacitive values thereof. This has the benefit of allowing the ESDP device to function effectively to protect a wide variety of entities that can comprise the internal circuitry characterizing the base semiconductor structure. So configuring the number vias to set the resistance and tune the ESDP device during fabrication of the semiconductor structure has advantages relating to economics and efficiency of fabrication.

Moreover, besides configuring the ESDP resistance with setting a particular number for the portion of the plurality of individual vias in parallel, embodiments

recited herein also allow the ESDP resistance to be configured with forming individual vias comprising the portion of the plurality of individual vias with a particular cross sectional area and/or forming the individual vias comprising the portion of the plurality of individual vias with a particular length.

Applicants have reviewed the Huang reference and find no teaching therein directed towards tuning an electrostatic discharge protective device for performing an electrostatic discharge protective function with the setting of a particular number of vias configured during fabrication, as recited in Claims 8, 16, 20 and 27 herein. Thus, for at least this reason, Applicants respectfully assert that the claimed embodiments recited herein are allowable over the cited reference under 35 USC 102(e).

Moreover, while Applicants respectfully agree with the Examiner that the structure taught by Huang would have more or less resistance depending upon the number of vias (OA at 5), the claimed embodiments herein recite an active tuning of the ESDP structure, so as to control its function, allowing it to protect any of a variety of internal circuits characterizing the semiconductor structure in which to is disposed. In contrast, Huang expressly teachings that (1) the multiple current carrying pathways therein allow smaller "line widths," which allow "more flexibility in circuit design" (Op. Cit. at ll. 52-54), and (2) that these allow continuing ESD protection even "when one of these [conductors] is *accidentally* severed" (Op Cit. at ll. 56-59) both implicitly teach away from the embodiments recited in Claim 8, 16, 20 and 27, wherein the ESDP resistance is configured during fabrication so as to tune the ESDP device.

For instance, Huang's "flexibility in circuit design" (Op. Cit.) implies improved versatility in conductor layout therein, as opposed to configurability of the ESDP's associated resistance to tune the ESDP device. Huang expressly reinforces this

implication in teaching that the ESDP taught therein remains functional after *accidental severing* of one of the conductors (Op. Cit.). Thus, in contrast to configuring a resistance value during fabrication from paralleled vias to purposefully tune the ESDP device, as recited herein, Huang's ESDP resistance does not depend upon a particularly configured resistance and/or upon a particularly configured number of vias. In fact, the change in resistance by *accidental severing* of one or more vias, as expressly taught by Huang, is inconsequential to the functioning of the ESD taught by Huang.

Applicants respectfully assert that this also teaches away from purposefully configuring ESDP resistance during fabrication to tune the ESDP, as recited in the claimed embodiments herein. Thus, Applicants respectfully assert that the Huang reference does not anticipate, teach or suggest the embodiments recited herein, nor provide motivation to produce such embodiments. For this additional reason, Applicants respectfully assert that Claims 8, 16, 20 and 27 and their respective dependent claims are allowable over the cited reference under 35 USC 102(e).

CONCLUSION

By the rationale stated above, Applicants respectfully assert that Claims 8, 16, 20 and 27 and their respective dependent claims are allowable over the cited reference under 35 USC 102(e). Applicants respectfully assert therefore that Claims 8-9, 16, 20-27 and 29-30 are in condition for allowance.

Accordingly, Applicants respectfully request that the rejection of Claims 8-9, 16, 20-27 and 29-30 under 35 U.S.C. 102(e) be withdrawn and that Claims 8-9, 16, 20-27 and 29-30 be allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

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